IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is set forth in the ensuing listing of the claims. This listing of the claims replaces all prior claims listings.

1. (Currently amended) A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over ~~said~~the active surface, ~~said~~the tape including at least one slot formed therethrough, each of ~~said~~the plurality of bond pads being exposed through ~~said~~the at least one slot, at least one end of ~~said~~the at least one slot extending beyond an outer periphery of ~~said~~the semiconductor die;

a substrate element positioned over ~~said~~the tape opposite ~~said~~the semiconductor die, ~~said~~the substrate element including a plurality of contact areas, each contact area of ~~said~~the plurality corresponding to a bond pad of ~~said~~the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through ~~said~~the substrate element and aligned with ~~said~~the at least one slot of ~~said~~the tape, ~~said~~the substrate element further including a contact pad in communication with each contact area of ~~said~~the plurality of contact areas by way of a substantially laterally extending conductive trace;

a quantity of encapsulant material substantially filling a volume defined by ~~said~~the at least one slot of ~~said~~the tape and ~~said~~the at least one opening of ~~said~~the substrate element; and

a coverlay secured to a surface of ~~said~~the substrate element opposite ~~said~~the tape, ~~said~~the coverlay substantially covering at least ~~said~~the at least one opening through ~~said~~the substrate element, contact pads of ~~said~~the substrate element being exposed beyond or through ~~said~~the coverlay.

2. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the plurality of bond pads is arranged substantially linearly along a central region of ~~said~~the active surface of ~~said~~the semiconductor die.

3. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the tape is formed from a material having a coefficient of thermal expansion similar to a coefficient of thermal expansion of a material of ~~said~~the semiconductor die.

4. (Currently amended) The semiconductor device package of claim 3, wherein ~~said~~the substrate element has a coefficient of thermal expansion similar to ~~said~~the coefficient of thermal expansion of ~~said~~the material of ~~said~~the semiconductor die.

5. (Currently amended) The semiconductor device package of claim 1, wherein both ends of ~~said~~the at least one slot formed through ~~said~~the tape extend beyond ~~said~~the outer periphery of ~~said~~the semiconductor die.

6. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the tape is adhesively secured to ~~said~~the active surface of ~~said~~the semiconductor die and to ~~said~~the substrate element.

7. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the substrate element comprises at least one of an interposer and a carrier substrate.

8. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the substrate element comprises silicon.

9. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the quantity of encapsulant material substantially encapsulates each intermediate conductive element.

10. (Currently amended) The semiconductor device package of claim 9, wherein ~~said~~the quantity of encapsulant material protrudes above a major plane of an exposed surface of ~~said~~the substrate element opposite ~~said~~the semiconductor die.

11. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the substrate element includes a recessed area adjacent ~~said~~the at least one opening, each contact area of ~~said~~the plurality of contact areas being located within ~~said~~the recessed area.

12. (Currently amended) The semiconductor device package of claim 11, wherein ~~said~~the quantity of encapsulant material substantially fills ~~said~~the recessed area.

13. (Currently amended) The semiconductor device package of claim 12, wherein ~~said~~the quantity of encapsulant material substantially encapsulates each ~~said~~the intermediate conductive element.

14. (Currently amended) The semiconductor device package of claim 12, wherein ~~said~~the quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of ~~said~~the substrate element.

15. (canceled)

16. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the coverlay comprises a recessed area within which each intermediate conductive element is contained.

17. (Currently amended) The semiconductor device package of claim 1, wherein ~~said~~the coverlay is secured to ~~said~~the substrate element with an adhesive material.

18. (Currently amended) The semiconductor device package of claim 17, wherein ~~said~~the adhesive material comprises a pressure sensitive adhesive material.

19. (Canceled)

20. (Currently amended) The semiconductor device package of claim 1, further comprising discrete conductive elements protruding from at least some of ~~said~~the contact pads.

21. (Currently amended) A semiconductor device assembly, comprising:

a semiconductor die with at least one bond pad on an active surface thereof;

a tape secured to ~~said~~the active surface, ~~said~~the tape including a slot formed therethrough with ~~said~~the at least one bond pad being exposed through ~~said~~the slot, at least one end of ~~said~~the slot extending beyond an outer periphery of ~~said~~the semiconductor die;

a substrate element positioned over ~~said~~the semiconductor die opposite ~~said~~the tape from ~~said~~the semiconductor die, ~~said~~the substrate element including at least one opening formed therethrough through which ~~said~~the at least one bond pad is exposed; and

a coverlay adhesively secured to a surface of ~~said~~the substrate element opposite ~~said~~the tape, ~~said~~the coverlay substantially covering at least ~~said~~the at least one opening through ~~said~~the substrate element.

22. (Currently amended) The assembly of claim 21, wherein ~~said~~the semiconductor die includes a plurality of bond pads arranged substantially linearly along a central region of ~~said~~the active surface.

23. (Currently amended) The assembly of claim 21, wherein ~~said~~the tape has a similar coefficient of thermal expansion to a coefficient of thermal expansion of ~~said~~the substrate element.

24. (Currently amended) The assembly of claim 23, wherein ~~said~~the semiconductor die has a similar coefficient of thermal expansion to ~~said~~the coefficient of thermal expansion of ~~said~~the substrate element.

25. (Currently amended) The assembly of claim 21, wherein two ends of ~~said~~the slot extend beyond ~~said~~the outer periphery of ~~said~~the semiconductor die.

26. (Currently amended) The assembly of claim 21, wherein ~~said~~the at least one end of ~~said~~the slot receives encapsulant material.

27. (Currently amended) The assembly of claim 25, wherein one of ~~said~~the two ends of ~~said~~the slot is positioned so as to facilitate displacement of air from ~~said~~the slot while an encapsulant material is being introduced at least into a volume defined by ~~said~~the slot from the other of ~~said~~the two ends.

28. (Currently amended) The assembly of claim 21, wherein ~~said~~the substrate element comprises at least one of an interposer and a carrier substrate.

29. (Currently amended) The assembly of claim 21, wherein ~~said~~the substrate element includes a recessed area formed adjacent ~~said~~the at least one opening in a surface of ~~said~~the substrate element located opposite ~~said~~the tape.

30. (Currently amended) The assembly of claim 29, wherein ~~said~~the substrate element includes at least one contact area corresponding to ~~said~~the at least one bond pad of ~~said~~the semiconductor die.

31. (Currently amended) The assembly of claim 30, wherein ~~said~~the at least one contact area is located within ~~said~~the recessed area.

32. (Currently amended) The assembly of claim 31, wherein ~~said~~the recessed area receives a portion of an intermediate conductive element that extends between ~~said~~the at least one bond pad and ~~said~~the at least one contact area.

33. (Currently amended) The assembly of claim 21, wherein ~~said~~the substrate element includes at least one contact area that corresponds to ~~said~~the at least one bond pad of ~~said~~the semiconductor die and at least one contact pad in electrical communication with ~~said~~the at least one contact area.

34. (Currently amended) The assembly of claim 33, further comprising at least one intermediate conductive element electrically connecting ~~said~~the at least one bond pad to ~~said~~the at least one contact area.

35. (Currently amended) The assembly of claim 34, wherein ~~said~~the at least one intermediate conductive element extends through ~~said~~the slot of ~~said~~the tape and ~~said~~the at least one opening of ~~said~~the substrate element.

36. (canceled)

37. (Currently amended) The assembly of claim 21, wherein ~~said~~the coverlay includes a recessed area configured to communicate with ~~said~~the at least one opening.

38. (Currently amended) The assembly of claim 37, wherein ~~said~~the recessed area is configured to receive a portion of at least one intermediate conductive element electrically connecting ~~said~~the at least one bond pad of ~~said~~the semiconductor die to a contact area on a surface of ~~said~~the substrate element adjacent ~~said~~the at least one opening formed therethrough.

39. (Currently amended) The assembly of claim 21, wherein ~~said~~the coverlay, ~~said~~the at least one opening formed through ~~said~~the substrate element, ~~said~~the slot formed through ~~said~~the tape, and ~~said~~the semiconductor die together form a receptacle.

40. (Currently amended) The assembly of claim 39, wherein ~~said~~the receptacle at least partially contains a quantity of encapsulant material.

41. (Currently amended) A method for packaging at least an active surface of a semiconductor die, comprising:

positioning a tape over the active surface so that at least one bond pad on the active surface is exposed through a slot formed through ~~said~~the tape and at least one end of ~~said~~the slot extends beyond an outer periphery of the semiconductor die;

positioning a substrate element over ~~said~~the tape so that ~~said~~the at least one bond pad is exposed through at least one opening formed through ~~said~~the substrate element and aligned with ~~said~~the slot, ~~said~~the substrate element including at least one contact area corresponding to ~~said~~the at least one bond pad;

electrically connecting ~~said~~the at least one bond pad to ~~said~~the at least one contact area;

adhesively securing a coverlay to an exposed surface of ~~said~~the substrate element to substantially cover ~~said~~the at least one opening formed through ~~said~~the substrate element; and

introducing encapsulant material through ~~said~~the at least one end into a receptacle formed by ~~said~~the coverlay, ~~said~~the at least one opening, ~~said~~the slot, and ~~said~~the semiconductor die from a location opposite the semiconductor die from ~~said~~the tape.

42. (Currently amended) The method of claim 41, wherein ~~said~~ positioning ~~said~~the tape comprises positioning over the semiconductor die a tape having a similar coefficient of thermal expansion to a coefficient of thermal expansion of the semiconductor die.

43. (Currently amended) The method of claim 42, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element having a similar coefficient of thermal expansion to ~~said~~the coefficient of thermal expansion of the semiconductor die.

44. (Currently amended) The method of claim 43, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning a substrate element comprising silicon over ~~said~~the tape.

45. (Currently amended) The method of claim 41, wherein ~~said~~ positioning ~~said~~the tape comprises orienting ~~said~~the slot with another end thereof extending laterally beyond ~~said~~the outer periphery of the semiconductor die.

46. (Currently amended) The method of claim 41, further including securing ~~said~~the tape to the active surface of the semiconductor die.

47. (Currently amended) The method of claim 46, wherein ~~said~~ securing comprises adhering ~~said~~the tape to the active surface.

48. (Currently amended) The method of claim 41, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning at least one of an interposer and a carrier substrate over ~~said~~the tape.

49. (Currently amended) The method of claim 41, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element comprising a recessed area adjacent ~~said~~the at least one opening and including therein ~~said~~the at least one contact area.

50. (Currently amended) The method of claim 49, wherein ~~said~~ introducing comprises introducing a portion of ~~said~~the encapsulant material into ~~said~~the recessed area.

51. (Currently amended) The method of claim 41, wherein ~~said~~ electrically connecting comprises connecting at least one intermediate conductive element between ~~said~~the at least one bond pad and ~~said~~the at least one contact area.

52. (Currently amended) The method of claim 51, wherein ~~said~~ connecting ~~said~~the at least one intermediate conductive element comprises wire bonding.

53. (Currently amended) The method of claim 51, wherein ~~said~~ connecting ~~said~~the at least one intermediate conductive element comprises extending ~~said~~the at least one intermediate conductive element through ~~said~~the slot formed through ~~said~~the tape and ~~said~~the at least one opening formed through ~~said~~the substrate element.

54. (Currently amended) The method of claim 41, wherein ~~said~~ positioning ~~said~~the coverlay comprises positioning over ~~said~~the substrate element a coverlay including a recessed area alignable over ~~said~~the at least one opening and over intermediate conductive elements extending through ~~said~~the at least one opening.

55. (Currently amended) The method of claim 41, further including securing ~~said~~the substrate element to ~~said~~the tape.

56. (Currently amended) The method of claim 55, wherein ~~said~~ securing comprises adhesively securing ~~said~~the substrate element to ~~said~~the tape.

57. (canceled)

58. (Currently amended) The method of claim 41, wherein ~~said~~ adhesively securing comprises securing ~~said~~the coverlay to ~~said~~the substrate element with a pressure sensitive adhesive.

59. (Currently amended) The method of claim 58, wherein ~~said~~ adhesively securing comprises removably securing ~~said~~the coverlay to ~~said~~the substrate element.

60. (Currently amended) The method of claim 41, wherein ~~said~~ introducing comprises substantially filling ~~said~~the slot formed through ~~said~~the tape and ~~said~~the at least one opening formed through ~~said~~the substrate element with ~~said~~the encapsulant material.

61. (Currently amended) The method of claim 41, wherein ~~said~~ introducing comprises substantially encapsulating at least one intermediate conductive element electrically connecting ~~said~~the at least one bond pad to ~~said~~the at least one contact area.

62. (Currently amended) The method of claim 41, wherein ~~said~~ positioning ~~said~~the coverlay comprises forming ~~said~~the receptacle, including ~~said~~the slot and ~~said~~the at least one opening, within which ~~said~~the at least one bond pad is located.

63. (Currently amended) A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, ~~said~~the tape including a slot through which at least one bond pad on the active surface of the semiconductor die

is exposed, at least a portion of ~~said~~the slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over ~~said~~the tape with at least one opening formed through ~~said~~the substrate element being located at least partially over ~~said~~the slot; and

adhesively securing a coverlay to ~~said~~the substrate element to substantially seal ~~said~~the at least one opening, ~~said~~the coverlay and lateral edges of ~~said~~the at least one opening and saidthe slot forming a receptacle.

64. (Currently amended) The method of claim 63, further comprising electrically connecting ~~said~~the at least one bond pad to at least one contact area located on a surface of ~~said~~the substrate element opposite ~~said~~the tape, proximate ~~said~~the at least one opening.

65. (Currently amended) The method of claim 64, wherein ~~said~~ electrically connecting comprises connecting at least one intermediate conductive element between ~~said~~the at least one bond pad and ~~said~~the at least one contact area.

66. (Currently amended) The method of claim 65, wherein ~~said~~ connecting ~~said~~the at least one intermediate conductive element comprises positioning ~~said~~the at least one intermediate conductive element at least partially within ~~said~~the slot and ~~said~~the at least one opening.

67. (Currently amended) The method of claim 63, wherein ~~said~~ positioning ~~said~~the tape comprises positioning a tape having a coefficient of thermal expansion similar to a coefficient of thermal expansion of the semiconductor die.

68. (Currently amended) The method of claim 67, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element having a coefficient of thermal expansion similar to ~~said~~the coefficient of thermal expansion of the semiconductor die.

69. (Currently amended) The method of claim 63, wherein ~~said~~ positioning ~~said~~the tape comprises positioning ~~said~~the tape with at least two regions of ~~said~~the slot extending laterally beyond ~~said~~the outer periphery of the semiconductor die.

70. (Currently amended) The method of claim 63, further comprising securing ~~said~~the tape to the active surface of the semiconductor die.

71. (Currently amended) The method of claim 70, wherein ~~said~~ securing comprises adhesively securing ~~said~~the tape to the active surface of the semiconductor die.

72. (Currently amended) The method of claim 64, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element including a recessed area adjacent at least a portion of an edge of ~~said~~the at least one opening, ~~said~~the at least one contact area being located within ~~said~~the recessed area.

73. (Currently amended) The method of claim 63, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element comprising at least one of an interposer and a carrier substrate.

74. (Currently amended) The method of claim 63, further comprising securing ~~said~~the substrate element to ~~said~~the tape.

75. (Currently amended) The method of claim 74, wherein ~~said~~ securing comprises adhesively securing ~~said~~the substrate element to ~~said~~the tape.

76. (Currently amended) The method of claim 63, wherein ~~said~~ positioning ~~said~~the coverlay comprises positioning over ~~said~~the substrate element a coverlay comprising a recess

formed therein, ~~said~~the recess being positioned so as to communicate with ~~said~~the at least one opening formed through ~~said~~the substrate element when ~~said~~ positioning is effected.

77. (canceled)

78. (Currently amended) The method of claim 63, wherein ~~said~~ adhesively securing comprises adhesively securing ~~said~~the coverlay to ~~said~~the substrate element with a pressure sensitive adhesive.

79. (Currently amended) The method of claim 63, wherein ~~said~~ securing comprises removably securing ~~said~~the coverlay to ~~said~~the substrate element.

80. (Currently amended) A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over ~~said~~the active surface, ~~said~~the tape including at least one slot formed therethrough, each of ~~said~~the plurality of bond pads being exposed through ~~said~~the at least one slot, at least one end of ~~said~~the at least one slot extending beyond an outer periphery of ~~said~~the semiconductor die;

a substrate element positioned over ~~said~~the tape opposite ~~said~~the semiconductor die, ~~said~~the substrate element including a plurality of contact areas, each contact area of ~~said~~the plurality corresponding to a bond pad of ~~said~~the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through ~~said~~the substrate element and aligned with ~~said~~the at least one slot of ~~said~~the tape, ~~said~~the substrate element further including a contact pad in communication with each contact area of ~~said~~the plurality of contact areas by way of a substantially laterally extending conductive trace;

a quantity of encapsulant material substantially filling a volume defined by ~~said~~the at least one slot of ~~said~~the tape and ~~said~~the at least one opening of ~~said~~the substrate element; and

a coverlay positioned over a surface of ~~said~~the substrate element opposite ~~said~~the tape, ~~said~~the coverlay substantially covering at least ~~said~~the at least one opening through ~~said~~the substrate element, contact pads of ~~said~~the substrate element being exposed through or beyond ~~said~~the coverlay.

81. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the plurality of bond pads is arranged substantially linearly along a central region of ~~said~~the active surface of ~~said~~the semiconductor die.

82. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the tape is formed from a material having a coefficient of thermal expansion similar to a coefficient of thermal expansion of a material of ~~said~~the semiconductor die.

83. (Currently amended) The semiconductor device package of claim 82, wherein ~~said~~the substrate element has a coefficient of thermal expansion similar to ~~said~~the coefficient of thermal expansion of ~~said~~the material of ~~said~~the semiconductor die.

84. (Currently amended) The semiconductor device package of claim 80, wherein both ends of ~~said~~the at least one slot formed through ~~said~~the tape extend beyond ~~said~~the outer periphery of ~~said~~the semiconductor die.

85. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the tape is adhesively secured to ~~said~~the active surface of ~~said~~the semiconductor die and to ~~said~~the substrate element.

86. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the substrate element comprises at least one of an interposer and a carrier substrate.

87. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the substrate element comprises silicon.

88. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the quantity of encapsulant material substantially encapsulates each intermediate conductive element.

89. (Currently amended) The semiconductor device package of claim 88, wherein ~~said~~the quantity of encapsulant material protrudes above a major plane of an exposed surface of ~~said~~the substrate element opposite ~~said~~the semiconductor die.

90. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the substrate element includes a recessed area adjacent ~~said~~the at least one opening, each contact area of ~~said~~the plurality of contact areas being located within ~~said~~the recessed area.

91. (Currently amended) The semiconductor device package of claim 90, wherein ~~said~~the quantity of encapsulant material substantially fills ~~said~~the recessed area.

92. (Currently amended) The semiconductor device package of claim 91, wherein ~~said~~the quantity of encapsulant material substantially encapsulates each ~~said~~the intermediate conductive element.

93. (Currently amended) The semiconductor device package of claim 91, wherein ~~said~~the quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of ~~said~~the substrate element.

94. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the coverlay comprises a recessed area within which each intermediate conductive element is contained.

95. (Currently amended) The semiconductor device package of claim 80, wherein ~~said~~the coverlay is secured to ~~said~~the surface of ~~said~~the substrate element.

96. (Currently amended) The semiconductor device package of claim 95, wherein ~~said~~the coverlay is secured to ~~said~~the surface of ~~said~~the substrate element with an adhesive material.

97. (Currently amended) The semiconductor device package of claim 96, wherein ~~said~~the adhesive material comprises a pressure sensitive adhesive material.

98. (Currently amended) The semiconductor device package of claim 80, further comprising discrete conductive elements protruding from at least some of ~~said~~the contact pads.

99. (Currently amended) A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, ~~said~~the tape including a slot through which at least one bond pad on the active surface of the semiconductor die is exposed, at least a portion of ~~said~~the slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over ~~said~~the tape with at least one opening formed through ~~said~~the substrate element being located at least partially over ~~said~~the slot; and

positioning a coverlay over ~~said~~the substrate element to substantially seal ~~said~~the at least one opening, ~~said~~the coverlay and lateral edges of ~~said~~the at least one opening and ~~said~~the slot forming a receptacle, contact pads ~~exposed to~~ at a surface of ~~said~~the substrate element

adjacent to which ~~said~~the coverlay is positioned being exposed through or beyond an outer periphery of ~~said~~the coverlay.

100. (Currently amended) The method of claim 99, further comprising electrically connecting ~~said~~the at least one bond pad to at least one contact area located on a surface of ~~said~~the substrate element opposite ~~said~~the tape, proximate ~~said~~the at least one opening.

101. (Currently amended) The method of claim 100, wherein ~~said~~ electrically connecting comprises connecting at least one intermediate conductive element between ~~said~~the at least one bond pad and ~~said~~the at least one contact area.

102. (Currently amended) The method of claim 101, wherein ~~said~~ connecting ~~said~~the at least one intermediate conductive element comprises positioning ~~said~~the at least one intermediate conductive element at least partially within ~~said~~the slot and ~~said~~the at least one opening.

103. (Currently amended) The method of claim 99, wherein ~~said~~ positioning ~~said~~the tape comprises positioning a tape having a coefficient of thermal expansion similar to a coefficient of thermal expansion of the semiconductor die.

104. (Currently amended) The method of claim 103, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element having a coefficient of thermal expansion similar to ~~said~~the coefficient of thermal expansion of the semiconductor die.

105. (Currently amended) The method of claim 99, wherein ~~said~~ positioning ~~said~~the tape comprises positioning ~~said~~the tape with at least two regions of ~~said~~the slot extending laterally beyond ~~said~~the outer periphery of the semiconductor die.

106. (Currently amended) The method of claim 99, further comprising securing ~~said~~the tape to the active surface of the semiconductor die.

107. (Currently amended) The method of claim 106, wherein ~~said~~ securing comprises adhesively securing ~~said~~the tape to the active surface of the semiconductor die.

108. (Currently amended) The method of claim 100, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element including a recessed area adjacent at least a portion of an edge of ~~said~~the at least one opening, ~~said~~the at least one contact area being located within ~~said~~the recessed area.

109. (Currently amended) The method of claim 99, wherein ~~said~~ positioning ~~said~~the substrate element comprises positioning over ~~said~~the tape a substrate element comprising at least one of an interposer and a carrier substrate.

110. (Currently amended) The method of claim 99, further comprising securing ~~said~~the substrate element to ~~said~~the tape.

111. (Currently amended) The method of claim 110, wherein ~~said~~ securing comprises adhesively securing ~~said~~the substrate element to ~~said~~the tape.

112. (Currently amended) The method of claim 99, wherein ~~said~~ positioning ~~said~~the coverlay comprises positioning over ~~said~~the substrate element a coverlay comprising a recess formed therein, ~~said~~the recess being positioned so as to communicate with ~~said~~the at least one opening formed through ~~said~~the substrate element when ~~said~~ positioning is effected.

113. (Currently amended) The method of claim 99, wherein ~~said~~ positioning ~~said~~ the coverlay includes securing ~~said~~ the coverlay to ~~said~~ the substrate element.

114. (Currently amended) The method of claim 113, wherein ~~said~~ securing comprises removably securing ~~said~~ the coverlay to ~~said~~ the substrate element.

115. (Currently amended) The method of claim 113, wherein ~~said~~ adhesively securing comprises removably securing ~~said~~the coverlay to ~~said~~the substrate element.

116. (Currently amended) The assembly of claim 21, wherein ~~said~~the coverlay is secured to ~~said~~the surface of ~~said~~the substrate element with an adhesive material.

117. (Currently amended) The assembly of claim 116, wherein ~~said~~the adhesive material comprises a pressure sensitive adhesive material.

118. (Currently amended) The assembly of claim 21, wherein ~~said~~the coverlay is removably secured to ~~said~~the surface of ~~said~~the substrate element.